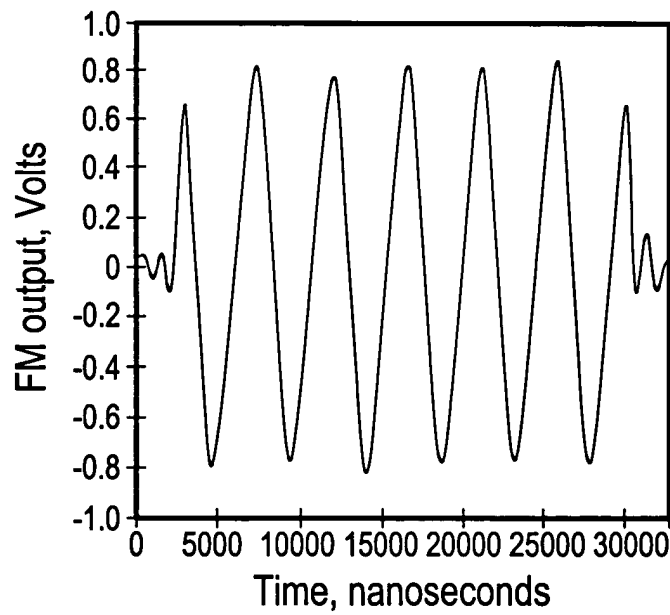
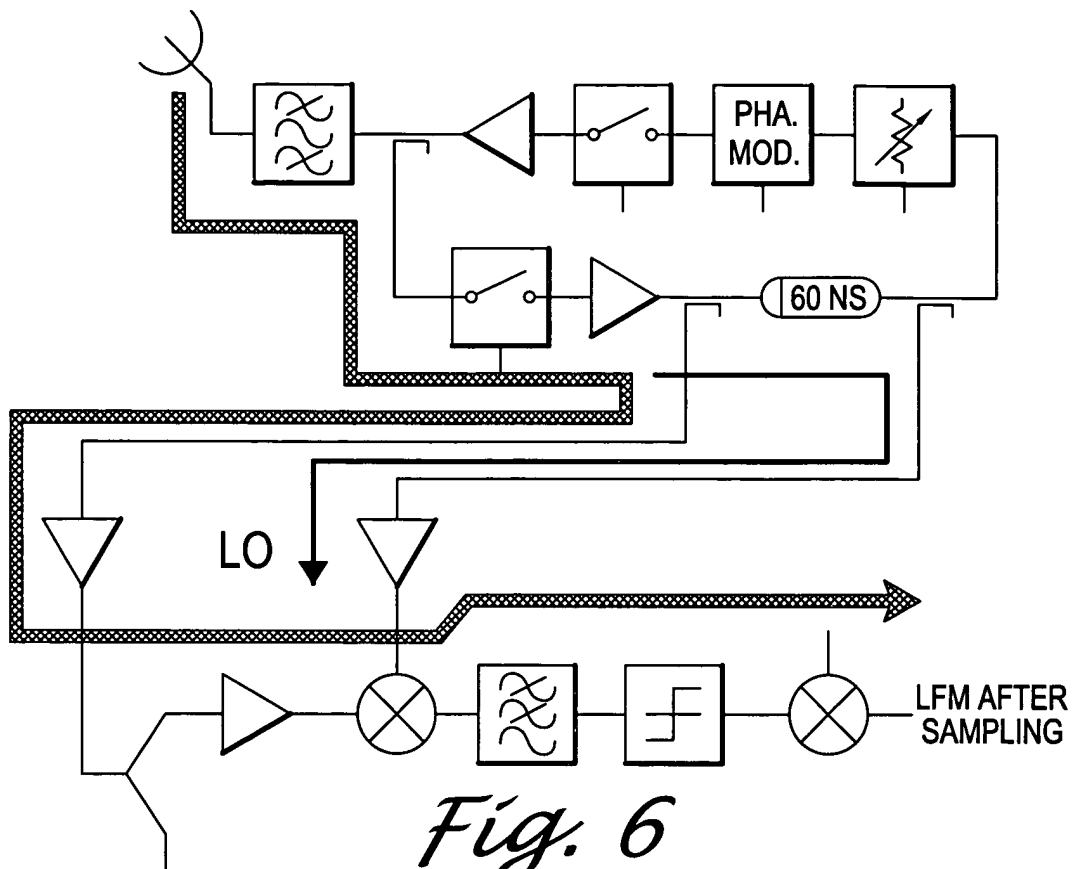


Fig. 5





```
TRANSITION = 0
CYCLES = 0
CYCLES_TEMP = 0
CLOCK = 2e6
FOR (n=2; n<=DATA; n++)
    IF ((SS[n] == 1) && (SS[n-1] == 1))
        CYCLES_TEMP = CYCLES_TEMP + 1
        CYCLES = CYCLES + 1
        IF (SLIN [n-1] != SLIN[n])
            TRANSITION = TRANSITION + 1
            CYCLES_TEMP = 1
        ELSE
            IF (TRANSITION == 0)
                CYCLES = 0
                CYCLES_TEMP = 0
            ELSE
                ELSE
CYCLES = CYCLES - CYCLES_TEMP
IF (CYCLES <= 0)
    CYCLES = 1
ELSE
FREQUENCY_ESTIMATE = (TRANSITION - 1) * CLOCK / (CYCLES * 2)
```

Fig. 7b

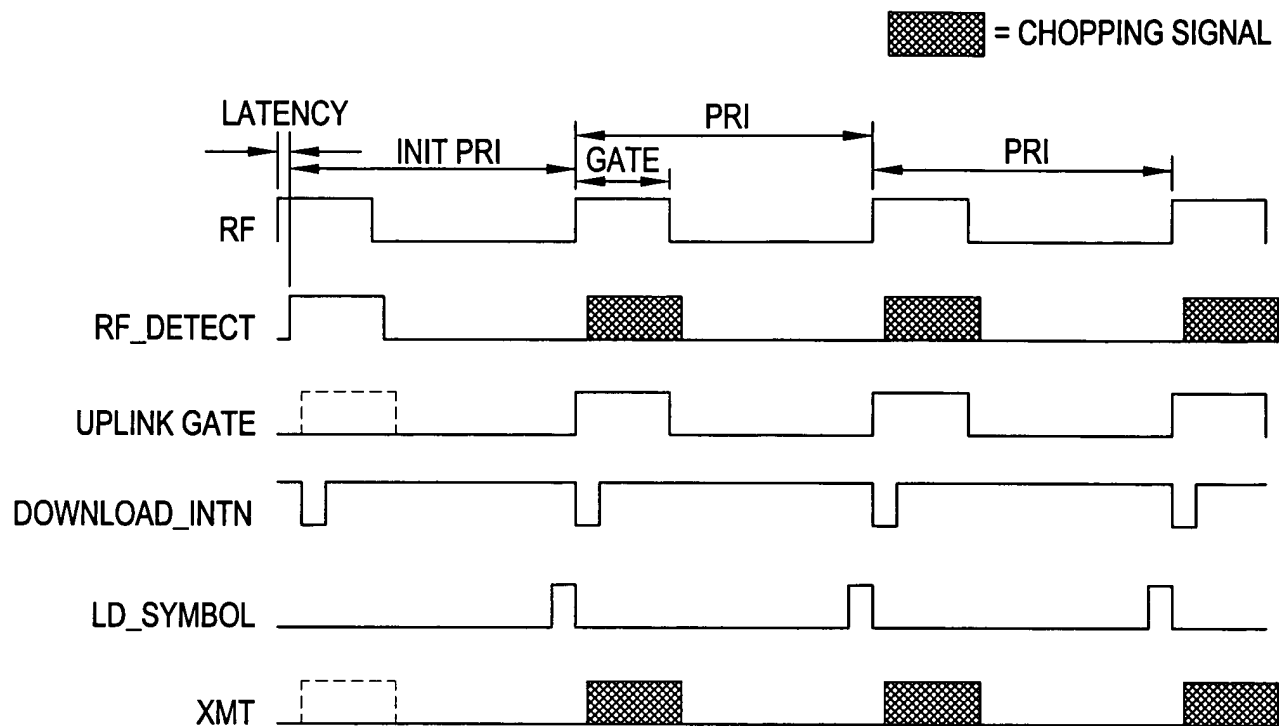
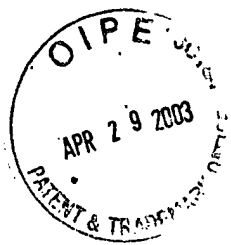


Fig. 8

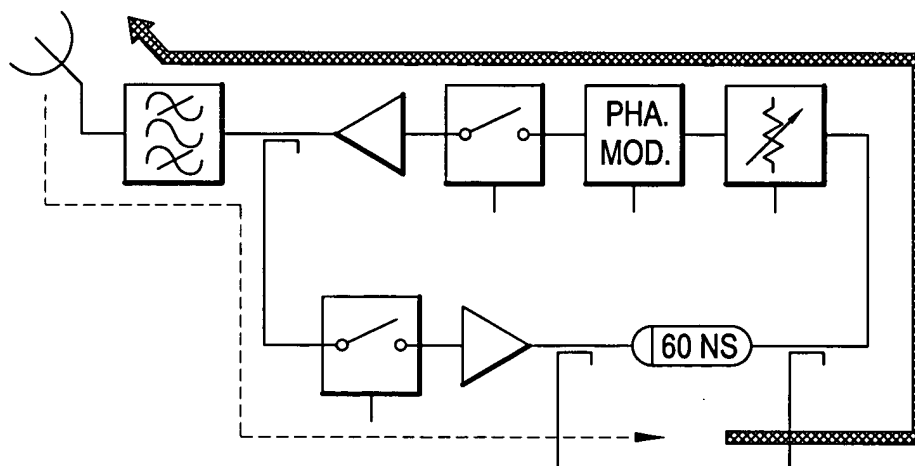


Fig. 9

NOTE: LOGIC HIGH IS SWITCH OPEN, LOGIC LOW IS SWITCH CLOSED.

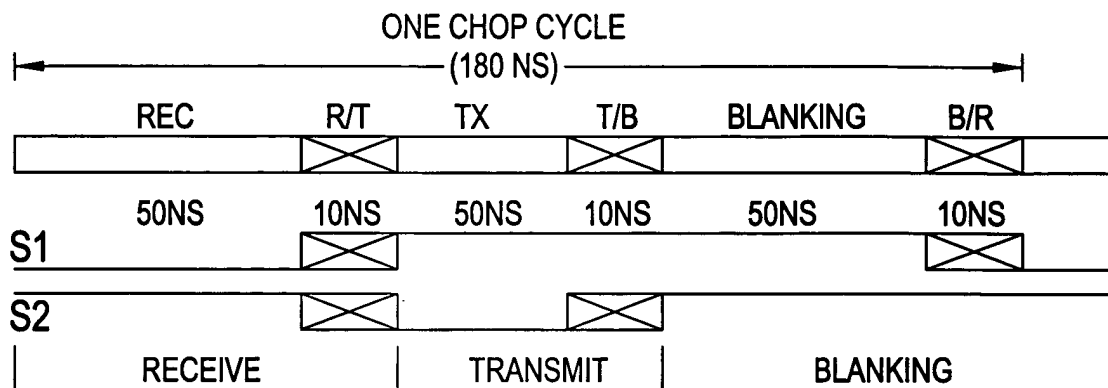


Fig. 10

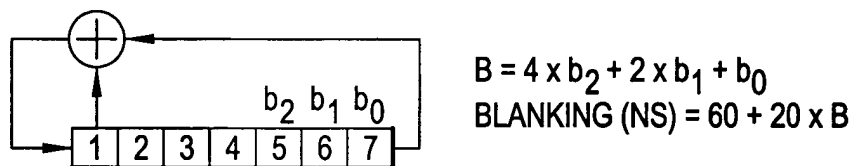


Fig. 11a

DATA BIT	AVERAGE FREQUENCY DEVIATION (HERTZ)	PHASE (DEGREES)
000	+3100586	+90
001	+1025391	+90
010	-3100586	+90
011	-1025391	+90
100	+3100586	-90
101	+1025391	-90
110	-3100586	-90
111	-1025391	-90

Fig. 11b

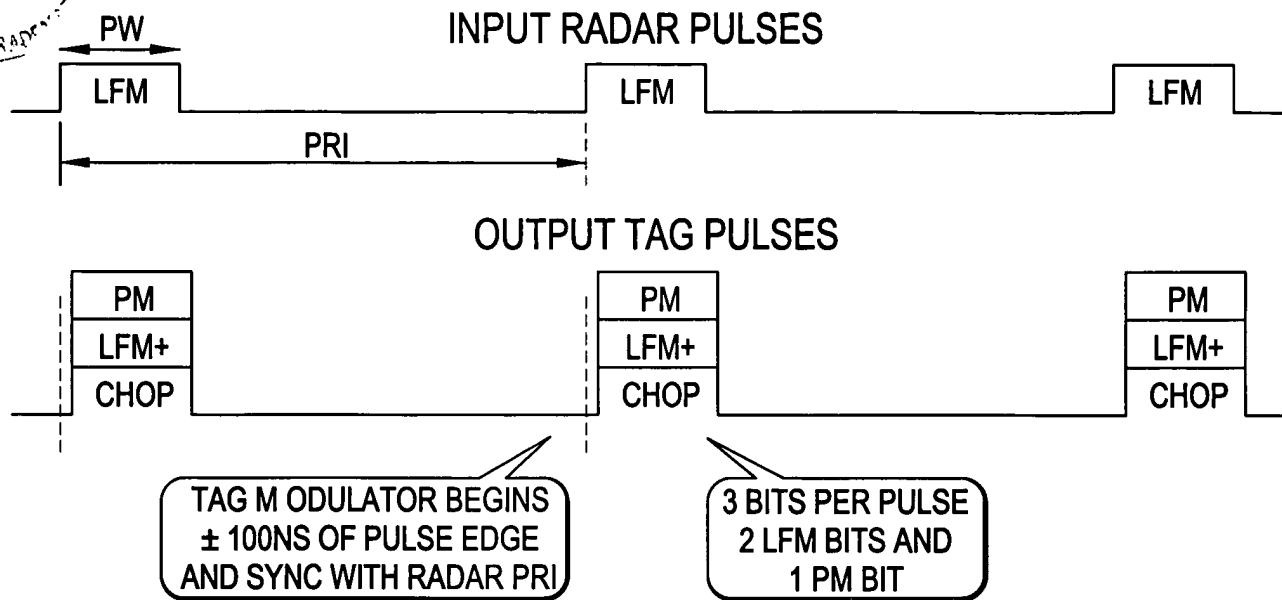


Fig. 12

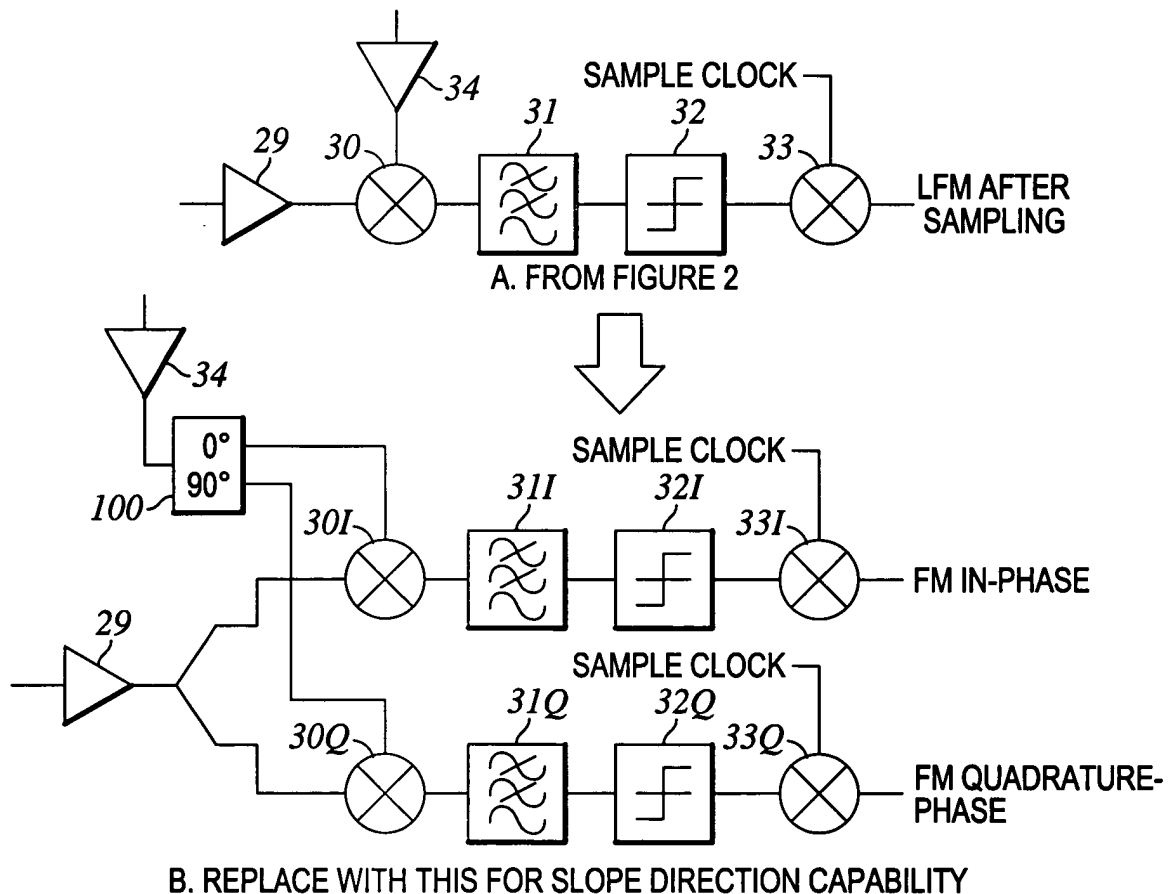


Fig. 13

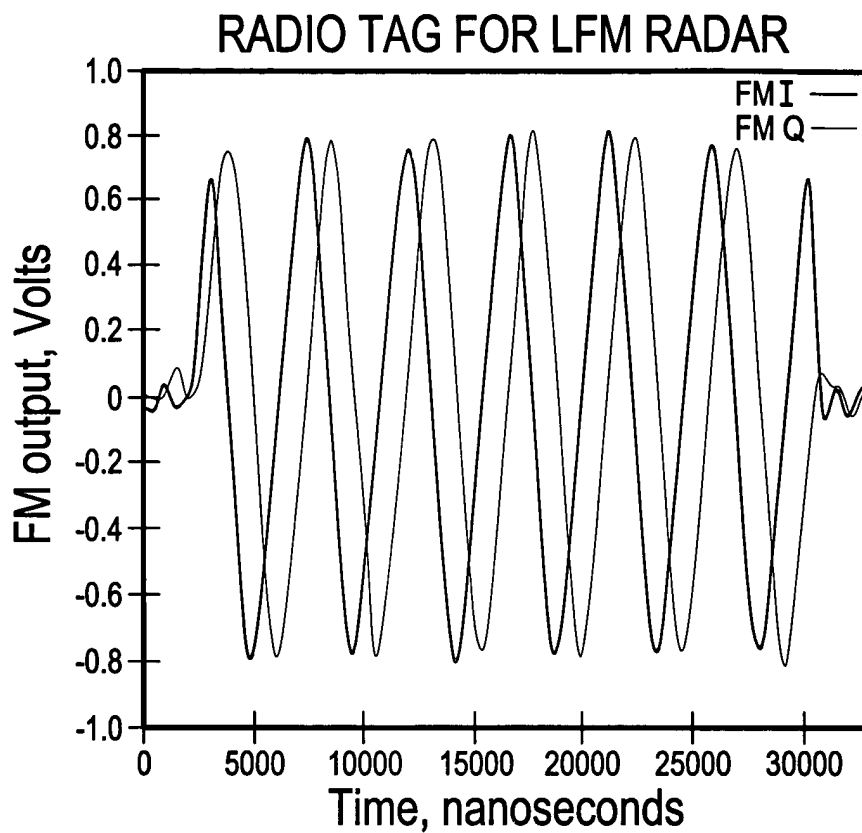


Fig. 14a

```
FOR (n = 2 ; N <= DATA ; n++)  
  IF ((SS[n] == 1) && (SS[n-1] == 1))  
    IF ((SLIN_Q[n-1] != SLIN_Q[n]) && SLIN_Q[n] == 1))  
      SLOPE[n] = SLIN_I[n]
```

Fig. 14b

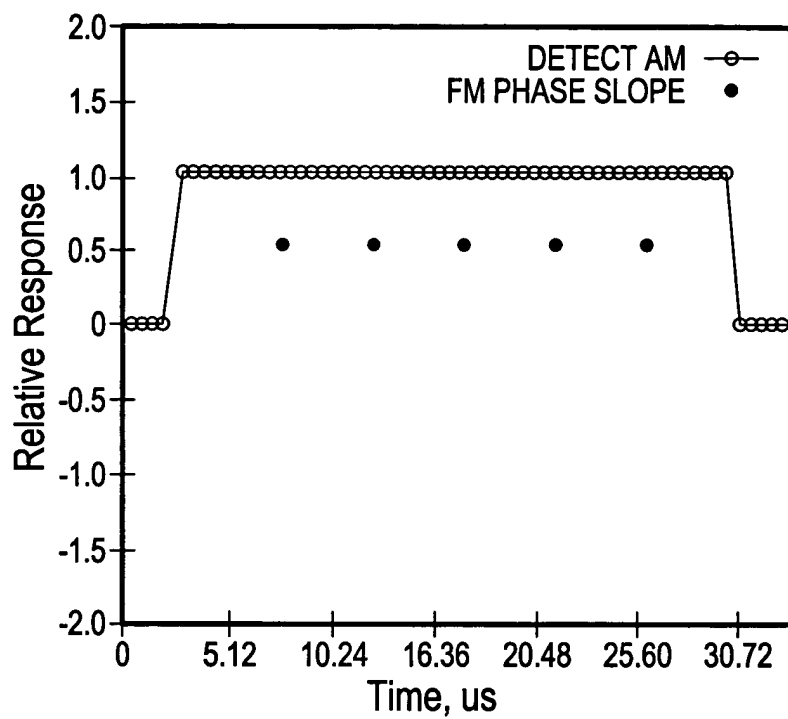


Fig. 15

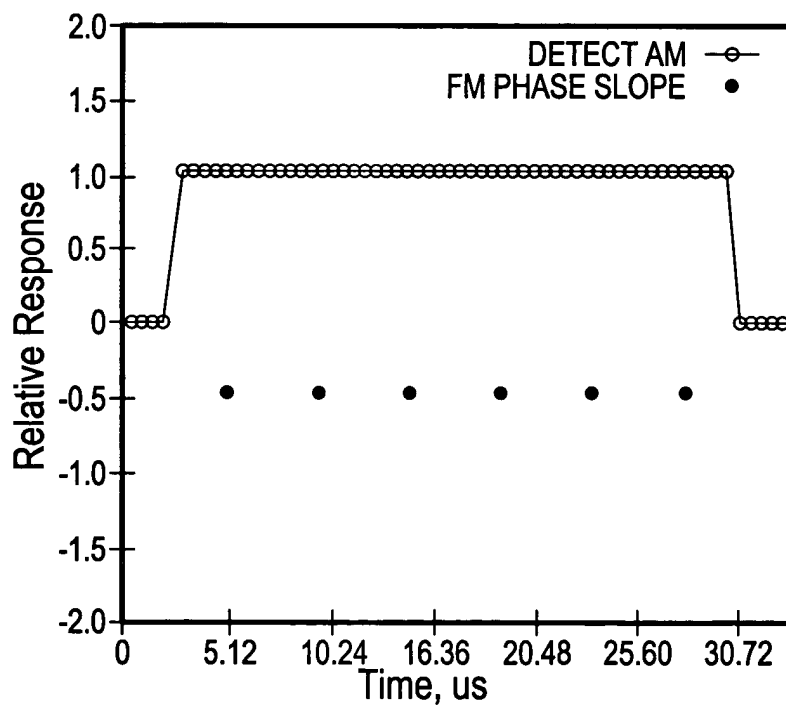
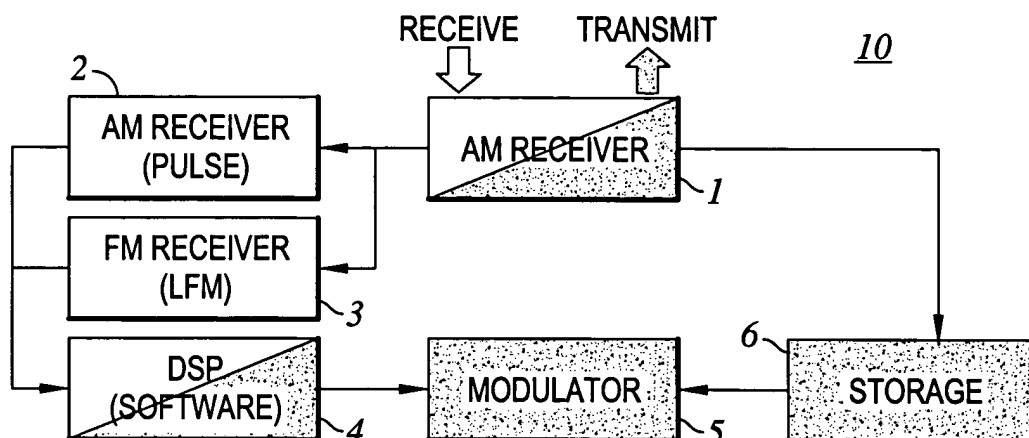


Fig. 16



The diagram illustrates a signal processing system. An input signal I is received by an antenna and passes through a filter 11. The output of filter 11 is split into two paths. The upper path contains a switch 20 controlled by $S2$, followed by a phase modulator 19 (labeled PHA. MOD.) and an amplitude modulator 18. The lower path contains a switch 13 controlled by $S1$, followed by a filter 14. The outputs of these two paths are combined at junction 15, then pass through a 60 NS delay element 16 to junction 17. The signal from junction 17 is split again. One branch goes through a filter 22 to junction 23. The other branch goes through a filter 34 to junction 30. At junction 23, the signal splits into two parallel processing chains. The upper chain consists of a filter 29, a multiplier 30, a filter 31, a square wave generator 32, and a multiplier 33. The lower chain consists of a filter 24, a diode 25, a filter 26, a filter 27, and an adder/subtractor 28. The output of the upper chain (multiplier 33) is labeled 'LFM AFTER SAMPLING'. The output of the lower chain (adder/subtractor 28) is labeled 'AM AFTER THRESHOLD SELECTOR'. A 'SAMPLE CLOCK' signal is provided to multiplier 33. A 'THRESHOLD' signal is provided to a DAC (Digital-to-Analog Converter) block 35, which is connected to the adder/subtractor 28.

Fig. 2

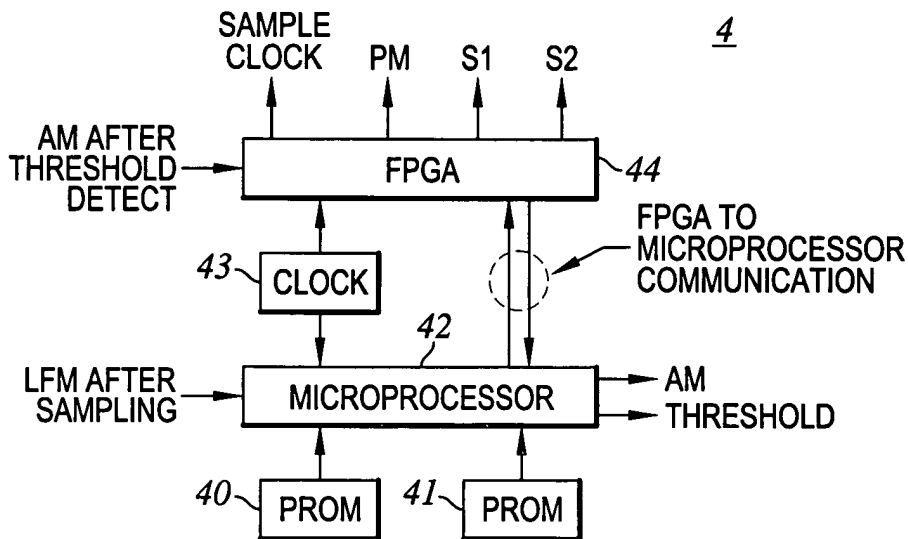


Fig. 3

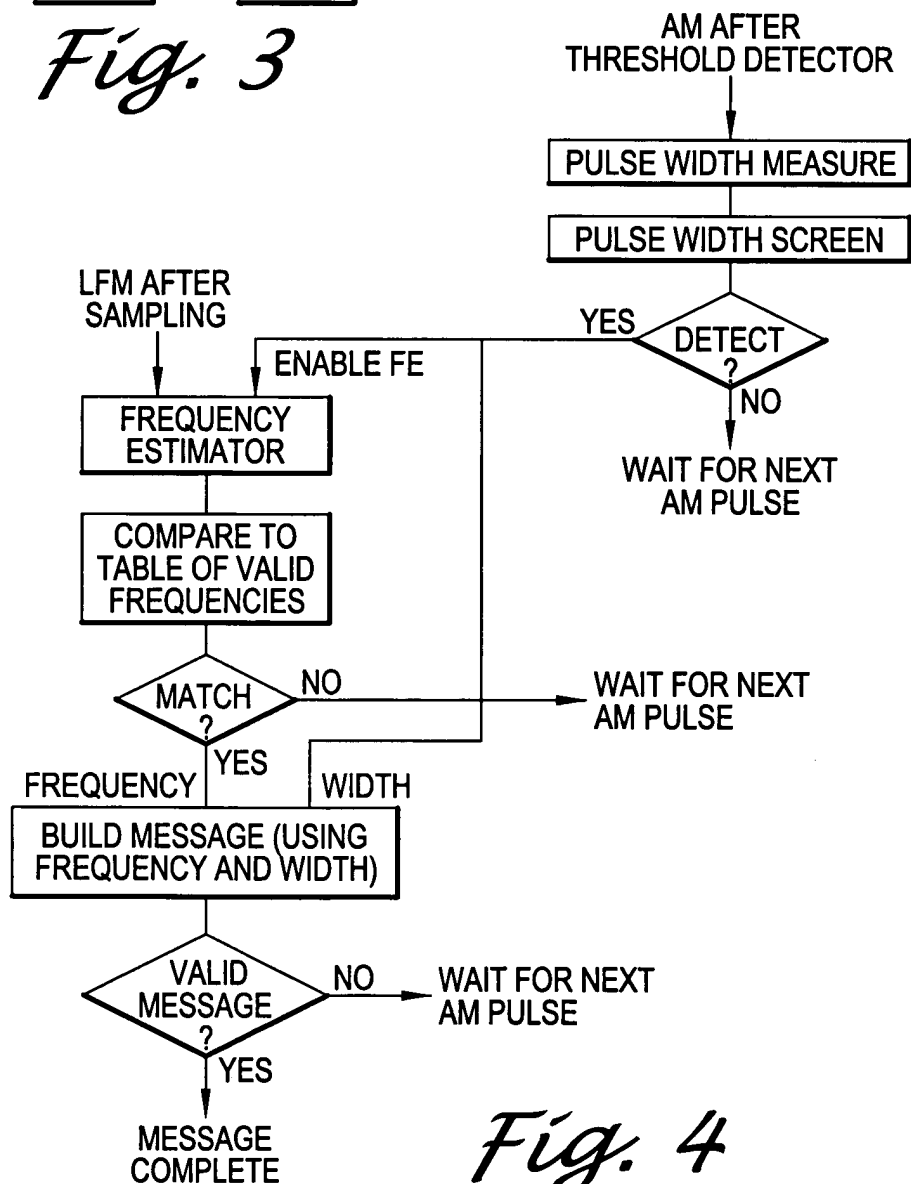


Fig. 4